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(54) Title: CONTENT ADDRESSED MEMORIES**(57) Abstract**

A content addressable memory comprises a CAM control logic unit (11) and a plurality of cells (10) connected in a chain. Each cell comprises a memory block (12) coupled to a common address bus (ADD), a comparator (14) coupled to a common data bus (DATA) and to the data interface of the memory block (12), switching means (15) coupling the data interface of the memory block with the data bus, and a logic block (13) including a Match flip-flop (16). The memory is operable in two phases, a Search phase and an Access phase. In the Search phase, a sequence of words on the common data bus (DATA) is serially matched with the contents of a sequence of addresses in the memory blocks (12) of the cells (10). In the Access phase, the cells matched in the Search phase are made serially available for access via the common address and data buses (ADD and DATA).

